What Is Claimed Is:

1. An electric circuit arrangement for controlling a solenoid-operated fluid valve,

- having an amplifier circuit, having an input stage and an output stage, which converts a voltage supplied to the input stage into a current of a corresponding magnitude, which flows from the output stage via connecting lines to a solenoid coil of the fluid valve,

wherein

- a monitoring circuit (19) having a current-measuring device (28) for the current (i_A) flowing from the output stage (12) via the connecting lines (15, 16) to the solenoid coil (17) is provided,

- the monitoring circuit (19) is supplied with a setpoint voltage (u_1) determining the magnitude of the current (i_A) flowing to the solenoid coil (17),

- the monitoring circuit (19) continuously reduces the voltage (u_2) supplied to the input stage (11) starting from the setpoint voltage (u_1) if the time average (u_{im}) of the current (i_A) has exceeded an upper threshold value (u_{io}), the monitoring circuit (19) interrupting a connecting line (15) leading to the solenoid coil (17) if the time average (u_{im}) of the current (i_A) has not fallen again below the upper threshold value (u_{io}) after a specifiable time, and

- the monitoring circuit (19) increases the voltage (u_2) supplied to the input stage (11) again to the setpoint voltage (u_1) after the time average (u_{im}) of the current (i_A) has fallen below the upper threshold value u_{io}.

2. The electric circuit arrangement as recited in Claim 1,
wherein

- a comparator (33) compares the time average (u_{im}) of the output signal (u_{iA}) of the current-measuring device (28) to an upper threshold value (u_{io}),

- the comparator (33) has an integration element (35) connected to it in outgoing circuit, the output voltage (u_{2k}) of which is limitable in such a way that it does not exceed an upper value (u_{2ko}),

- the output voltage (u_{2k}) of the integration element (35) decreases for as long as the time average (u_{im}) of the current (i_A) exceeds the upper threshold value (u_{io}), and the output voltage (u_{2k}) of the integration element (35) increases for as long as the time average (u_{im}) of the current (i_A) is less than the upper threshold value (u_{io}),

- the output voltage (u_{2k}) of the integration element (35) and the setpoint voltage (u_1) are supplied to a minimum value selection element (36) and

- the smaller (u_2) of the two voltages of the input stage (11) is supplied to the amplifier circuit (10).

3. The circuit arrangement as recited in Claim 2,
wherein the upper value (u_{2ko}) is limitable to the output voltage (u_{2k}) of the integration element (35), at least equal to the maximum setpoint voltage ($u_{1[100\%]}$).

4. The circuit arrangement as recited in Claim 2 or Claim 3,
wherein the time average (u_{im}) of the current (i_A) is supplied to the comparator (33) via a time-delay element (32).

5. The circuit arrangement as recited in one of Claims 2 through 4,
wherein an absolute-value generator (31) is connected between the current-measuring device (28) and the comparator (33).

6. The circuit arrangement as recited in one of Claims 2 through 5,
wherein

- the output voltage (u_{2k}) of the integration element (35) and a voltage corresponding to a lower threshold value (u_{2u}) are supplied to the inputs of a second comparator (38) and

- the second comparator (38) controls a relay (21) having a switching contact (K_{11}), the switching contact (K_{11}) interrupting a connecting line (15) if the output voltage (u_{2k}) of the integration element (35) has become smaller than the lower threshold value (u_{2u}).

7. The circuit arrangement as recited in Claim 6,
wherein the second comparator (38) controls a second relay (22) having a switching

contact (K_{21}), the switching contact (K_{21}) interrupting the other connecting line (16) if the output voltage (u_{2k}) of the integration element (35) has become smaller than the lower threshold value (u_{2u}).

8. The circuit arrangement as recited in Claim 6 or Claim 7,
wherein

- a bistable switch (39) is situated between the second comparator (38) and the relay(s) (21, 22).

- the second comparator (38) switches the bistable switch (39) from a first position into a second position if the output voltage (u_{2k}) of the integration element (35) has become smaller than the lower threshold value (u_{2u}), and

- the bistable switch (39) in the first position is reset by a separate reset signal.

9. The circuit arrangement as recited in Claim 8,
wherein the second comparator (38) and the bistable switch (39) are configured as a comparator (40) having a self-holding mechanism.

10. The circuit arrangement as recited in one of Claims 2 through 9,
wherein

- in an amplifier circuit (10*) controlling two solenoid coils (17, 44), which controls the one solenoid coil (17) in the case of a positive setpoint voltage ($+u_1$) and the other solenoid coil (44) in the case of a negative setpoint voltage ($-u_1$), the minimum value selection element (36*) while preserving the sign of the setpoint voltage (u_1) selects the smaller value in terms of absolute value and supplies it to the amplifier circuit (10*) as an input voltage (u_2),

- a computing element (55) forms the sum (u_{iS}) of the voltages (u_{iA}, u_{iB}) corresponding to the currents (i_A, i_B) flowing across the solenoid lines (15 and 16 or 45 and 46) and

- the sum signal (u_{iS}) is supplied to the first comparator (33).

11. The circuit arrangement as recited in Claim 10 having two relays (21, 22) controlled by the second comparator (38),
wherein each relay (21, 22) in each instance interrupts one of the connecting lines (15,

16, 45, 46) leading to the solenoid coils (21, 22) if the output voltage (u_{2k}) of the integration element (35) has become smaller than the lower threshold value (u_{2u}).